ABSTRACT

A method and system for providing an interconnect on a semiconductor device is disclosed. The method and system comprises providing a semiconductor substrate with a plurality of device structures thereon and providing at least one slot in the semiconductor substrate. The method and system include providing a metal within the at least one slot.

This first metal in a preferred embodiment consists of three depositions of metal when sputtered, with the first two depositions being buried in the silicon prior to a dielectric and a third deposition of what is called the first metal layer. This third deposition provides the normal interconnect pattern as it normally is patterned in standard metalization schemes.

In a preferred embodiment, the interconnect consists of a combination of a buried power buss and interconnect layer that, when employed properly, provides the following advantages:

1. Slotted metal having an oxide jacket surrounding it, thus allowing the metal to be connected randomly while isolating itself from other circuit functions.

2. Low interconnect sheet resistance available per function performed.

3. Low Ron X Area for a given area, where Ron is the on resistance of a Bipolar Transistor, or an MOS transistor (when used in a CMOS or BiCMOS configuration).

4. Provides an oxide isolated ground strap that is an ideal short to ground.

5. Provides ground strap throughout the integrated circuit wherever isolation is required between components.

6. Provides a metalized sinker for connecting the collector of a BiPolar transistor to the buried layer, or a metalized drain for connecting the drain to the buried layer of a CMOS device; thus ensuring the lowest collector or drain resistance.

7. Provides a metalized sinker and ground strap while eliminating the masking

and long time, high temperature isolation diffusion that is in standard processing.

8. Provides a metalized sinker and ground strap while eliminating the masking and long time, high temperature sinker diffusion.

9. When the epitaxial layer is less than 6 microns thick it allows the buried layer masking to be eliminated.

10. Oxide isolation in place of junction isolation results in lower leakage and lower capacitance thus providing a method for improved performance of high frequency, low power devices.

11. Low interconnect sheet resistance that allows for reduced interconnect RC time constants and therefore faster operation.

12. Low interconnect sheet resistance for high current, high power operation of integrated circuits.

13. Significant improvement in heat transfer over standard or damascene methods of metalization and interconnect.

14. Reduced current density in critical parts of the operation of the integrated circuit over standard approaches and other approaches used at this time.

15. Improved electromigration by an order of magnitude due to the improvement in heat transfer and reduced current density.

16. Elimination of isolation and sinker processes in integrated circuits.

17. Significant reduction in the die size for a given function since the isolation and sinker are provided by the buried power buss which is oxide isolated; thus allowing the isolation and sinker to move much closer to other active areas of Bipolar, MOS, DMOS, CMOS and passive components.

18. Significant reduction in de-biasing of emitter, collector, drain in high current applications due to the increase of cross section of metal through the use of this buried power buss. This results not only in a higher gain in these active circuit components, but also wider current range.

19. More gross die per wafer due to the reduction of die size and other savings. Since defect density is a function of area this approach results in less defects due to the reduction in the area of the die and higher yield. This combination of more die per wafer and lower yield loss results in more net die per wafer for a given function when using the buried power buss.

20. Due to improvement in de-biasing, the improvement in heat transfer, and the smaller die; the resulting die is viable in a smaller package and therefore opens up new markets.

21. All these functions and improvements are provided by a single masking process that provides the slots that are oxidized and metalized, while dropping process steps that are numerous, long in process time, and at high temperatures. This results in an integrated circuit process that is very low in Root Dt (square root of the diffusion constant times time). It is a proven fact that processes carried on at lower temperatures reduces the chance for defect introduction and propagation.

22. Due to the improved heat transfer, die using this approach are able to work at higher power dissipation before being limited by secondary breakdown.

23. Due to the thicker metal in the bonding pads there is increased protection against ESD failures as well as providing an improved bonding reliability.

24. The buried power buss is able to supply thick low sheet resistance metal to

both the emitter and collector on Bipolar power devices to prevent de-biasing and provide low Ron resistance of the power output transistor.